1. (Original) A programmable wire structure for an integrated circuit, comprising:

a programmable switch coupling two nodes, said switch having a first state that connects said two nodes, and said switch having a second state that disconnects said two nodes; and

a configuration circuit coupled to said programmable switch, said circuit comprising a means to program said switch between said first and second state; and

a first metal layer fabricated above a silicon substrate layer, said switch and said configuration circuit fabricated substantially above said first metal layer.

2. (Original) The structure of claim 1, wherein a second metal layer is fabricated substantially above said switch and said configuration circuit.

3. (Original) The structure of claim 1, wherein at least one of said first and second nodes is coupled to a node in said first metal.

4. (Original) The structure of claim 2, wherein at least one of said first and second nodes is coupled to a node in said second metal.

5. (Original) The structure of claim 1, wherein said programmable switch comprises a thin film transistor.

6. (Original) The structure of claim 5, wherein at least one of said first and second nodes of said programmable switch further comprises a via structure, said via structure containing a seed metal, said seed metal facilitating a thermally activated phase change of at least one of said thin

film materials to improve conduction of said connect state.

7. (Original) The structure of claim 1, wherein said configuration circuit comprises a thin film transistor.

8. (Original) The device of claim 1, wherein said configuration circuit comprises a memory element.

9. (Original) The structure of claim 8, wherein said memory element is selected from one of fuse links, anti-fuse capacitors, SRAM cells, DRAM cells, metal optional links, EPROM cells, EEPROM cells, flash cells, ferro-electric elements, electro-chemical elements, optical elements and magnetic elements.

10. (Previously Amended) The structure of claim 8, wherein the programmable switch further comprises:

a pass-gate device, said pass-gate controlled by an output signal from said memory element, said first state generated by an on pass-gate, and said second state generated by an off pass-gate; and

a configuration access to program said memory data, said memory bit polarity generating an on and off control signal to select said state of pass-gate device.

11 – 22 (Deleted)

23. (Currently amended) A semiconductor device for integrated circuits with two selectable manufacturing configurations, comprising:

a first module layer having an array of structured cells, said module layer having at least one layer of metal; and

a second module layer formed substantially above said first module layer comprising two selectable configurations, wherein:

in a first selectable configuration a programmable interconnect structure is formed to connect said structured cells, and

in a second selectable configuration a customized interconnect structure is formed to connect said structured cells;

wherein, said programmable interconnect structure is further comprised of a user configurable memory circuit constructed on a thin film layer comprising one of fuse links, anti-fuse capacitors, SRAM cells, DRAM cells, metal optional links, EPROM cells, EEPROM cells, flash cells, ferro-electric elements, electro-chemical elements, optical elements and magnetic elements; and

~~The device of claim 22,~~ wherein, said customized interconnect structure is further comprised of ~~said~~ ((a)) conductive pattern comprising fabricating hard wire controls to replicate a specific memory pattern, wherein replicating comprises:

a logic zero memory output mapped to a hard wire disconnect; and

a logic one memory output mapped to a hard wire connect.